## IN THE CLAIMS

1. (original) A system comprising:

a host/data controller; and

a memory system comprising a plurality of memory cartridges operably coupled to the host/data controller, each memory cartridge comprising an operation indicator configured to indicate the operational status of the corresponding memory cartridge.

2. (original) The system, as set forth in claim 1, wherein the memory system comprises a redundant memory system.

3. (original) The system, as set forth in claim 2, wherein the memory system comprises five memory cartridges.

4. (original) The system, as set forth in claim 3, wherein the operation indicator comprises a bit having a first state and a second state, the first state indicating that the memory cartridge is operational and the second state indicating that the memory cartridge is not operational.

5. (original) The system, as set forth in claim 4, wherein the memory system is configured to operate in a redundant mode when each of the bits is in the first state.

6. (original) The system, as set forth in claim 5, wherein at least one of the host/data controller and the plurality of memory cartridges comprise error detection components.

7. (original) The system, as set forth in claim 6, wherein the host/data controller is configured to generate a low priority interrupt signal in response to error detection by the error detection components if each of the operation bits is in the first state.

8. (original) The system, as set forth in claim 6, wherein the host/data controller is configured to generate a low priority interrupt signal in response to multi-bit error detection by the error detection components if each of the operation bits is in the first state.

9. (original) The system, as set forth in claim 6, wherein the host/data controller is configured to generate a high priority interrupt signal in response to multi-bit error detection if at least one of the operation bits is in the second state.

10. (original) The system, as set forth in claim 1, wherein each of the plurality of memory cartridges comprises a plurality of memory devices.

11. (original) A method of generating interrupts in a redundant memory, comprising the acts of:

detecting an error in a memory system;

determining the operational status of the memory system; and

initiating a system interrupt signal, the type of system interrupt signal being dependent on the operational status of the memory system.

12. (original) The method, as set forth in claim 11, wherein the act of detecting an error comprises the act of detecting a multi-bit error.

13. (original) The method, as set forth in claim 11, wherein the act of determining the operational status comprises the act of determining whether the system is operating in one of a redundant mode and a non-redundant mode.

14. (original) The method, as set forth in claim 13, wherein the act of determining the operational status comprises reading a plurality of operation bits, each of the operation bits indicating the operational status of a corresponding segment of the memory, the operational status comprising one of an operational state and a non-operational state.

15. (original) The method, as set forth in claim 14, wherein the act of determining the operational status comprises reading five operation bits.

16. (original) The method, as set forth in claim 15, wherein the act of initiating a system interrupt comprises the act of initiating a low priority system interrupt if each of the five operation bits is in the operational state.

17. (original) The method, as set forth in claim 15, wherein the act of initiating a system interrupt comprises the act of initiating a high priority system interrupt if any of the five operation bits is in the non-operational state.

Claims 18-91 (cancelled).